CLAIMS:

1. A processing apparatus for implementing a systolic-array-like structure, said apparatus comprising:

a) input means for inputting data;

b) register means (DCF) for storing said input data in a predetermined sequence;

c) processing means (FU) for processing d ta received from said register means (DCF) based on control signals generated from instruction data; and

d) register control means for controlling the depth of said register means (DCF) in accordance with said instruction data.

2. An apparatus according to claim 1, wherein said register means comprises distributed register files (DCF) provided at input terminals of a plurality of functional units (FU) of said processing means.

3. An apparatus according to claim 2, wherein said distributed register files (DCF) comprise depth-configurable FIFO register files addressable for individual registers.

4. An apparatus according to claim 3, wherein said register control means are arranged to determine the last logical register (R) of said FIFO register files (DCF) based on control signals derived from said instruction data.

5. An apparatus according to any of the preceding claims, further comprising at least one issue slot (I1 to I4) for storing said instruction data.

6. An apparatus according to claim 5, wherein said register control means are arranged to use a part of the bit pattern of said instruction data stored in said at least one issue slot (I1 to I4) for controlling said depth of said register means.

7. An apparatus according to any one of the preceding claims, wherein said programmable processing apparatus is a scalable VLIW processor or a coarse-grained reconfigurable processor.

8. An apparatus according to any one of claims 2 to 7, wherein said distributed register files (DCF) are connected to an interconnect network made up of a plurality of point-to-point connection lines.

9. An apparatus according to claim 8, wherein said point-to-point interconnect lines have a single source.

10. An apparatus according to claim 8, wherein said interconnect network is partially connected.

11. A processing method for implementing a systolic-array-like structure, said method comprising:

a) storing said input data in a register file (DCF) in predetermined sequence;

b) processing data received from said register file based on control signals generated from instruction data; and

c) controlling the depth of said register file (DCF) in accordance with said instruction data.